Amendments to the Specification

Please replace the paragraph at page 5, lines 8 through 17 with the following amended paragraph:

Referring again to FIG. 1, the echo logic interface 24 is configured to receive the TD_Bypass signal from the echo canceller unit 26 and store the TD_Bypass signal in an internal 32 bit register. The echo logic ~~signal~~ interface 24 produces the Overall Bypass signal by performing a logical OR upon the received TD_Bypass signal, and an alternative bypass signal generated by CPU 28. The Overall Bypass signal is clocked to the echo canceller unit 26 at the channel time-division rate. In this manner, echo cancellation on each of the channels is determined by the TD_Bypass signal and by the alternative bypass signal, so that the CPU 28 can direct that echo cancellation be disabled on any channel independently of the tone disabler circuit of the echo canceller unit.